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PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

August 1, 2006 — Date

Alexandra Beggs — Alexandra Beggs

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | | |
|---|---|---|
| Applicants | : Brian W. Huber and David R. Brown | Attorney Docket No.: 500125.02 |
| Patent No. | : US 6,815,994 B2 | |
| Issued | : November 9, 2004 | |
| Title | : METHOD OF SCALING DIGITAL CIRCUITS AND CONTROLLING THE TIMING RELATIONSHIP BETWEEN DIGITAL CIRCUITS | |

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## NOTIFICATION OF ERRORS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The following errors were noted in a review of the above-identified letters patent. One or more of these errors was inadvertently made in the original application, while the others occurred in the printing of the patent. Since the errors are of an obvious nature, a formal Certificate of Correction is not believed to be warranted at this time. Therefore, applicants request that this notification be placed in the Patent and Trademark Office file.

| Column, Line | Reads | Should Read |
|---|---|---|
| Item (56), IBM Reference | "IBM, "*Method of Deskewing Data Pulses*," IBM Technical Disclosure Bulletin, vol. 28, No. 6, Nov. 1985, ppl. 2658- | IBM, "*Method of Deskewing Data Pulses*," IBM Technical Disclosure Bulletin, vol. 28, No. 6, Nov. 1985, pp. 2658-2659." |

| | | |
|---|---|---|
| | 2659." | |
| Item (57), Lines 2, 6 and 9 | "complimentary" | --complementary-- |
| Column 1, Line 41 | "incoming clock signal," | --incoming clock signals,-- |
| Column 2, Line 16 | "The high-speed" | --The high speed-- |
| Column 2, Line 43 | "second complimentary" | --second complementary-- |
| Column 3, Line 24 | "modifications" | --modification-- |
| Column 4, Line 25 | "a PMOS transistors" | --a PMOS transistor-- |
| Column 5, Line 18 | "In this is faster" | --It is this faster-- |
| Column 5, Line 21 | "illustrated FIG. **2**" | --illustrated in FIG. **2**-- |
| Column 5, Line 59 | "of FIG. **6,**" | --of FIG. **6**-- |
| Column 7, Line 37 | "complimentary" | --complementary-- |
| Column 8, Line 63 | "portion or the circuitry" | --portion of the circuitry-- |

Respectfully submitted,

Date: July 31, 2006

By: Edward W. Bulchis

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Enclosure:
Postcard